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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,547	09/09/2003	Sheng Teng Hsu	SLA 0746	3059

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SHARP LABORATORIES OF AMERICA, INC
5750 NW PACIFIC RIM BLVD
CAMAS, WA 98642

EXAMINER	
PERKINS, PAMELA E	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,547	HSU ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13-19 and 21-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13-19 and 21-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the RCE on 6 April 2006 and the petition decision on 10 October 2006. Claims 1-3, 5-11, 13-19 and 21-27 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 11, 21, 23, 24 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al. (6,548,342).

Referring to claims 1, 5, 24 and 26, Suzuki et al. disclose a ferroelectric transistor where source, drain, and channel regions are formed in a substrate (44) (Fig. 6); a gate structure including: a conductive oxide layer (43), consisting of RuO, overlying the channel region; a ferroelectric material layer (42) overlying the conductive oxide layer (43); and, a top electrode conductive layer (41) overlying the ferroelectric material layer (42) (Fig. 4; col. 9, lines 29-60).

Referring to claims 3 and 11, wherein the electrode conductive layer (43) is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide (col. 9, lines 29-60).

Referring to claim 21, wherein the conductive oxide layer overlying the channel region having a lattice structure; the ferroelectric material layer overlying the conductive oxide layer having a lattice structure matching the conductive oxide lattice structure (col. 1, line 48 thru col. 2, line 14).

Referring to claim 23, wherein the ferroelectric material layer has a perovskite crystal lattice structure col. 1, lines 48-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6, 22, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Willer et al. (6,538,273).

Suzuki et al. disclose the subject matter claimed above except a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a method of fabricating a ferroelectric transistor where a gate stack is formed on a semiconductor substrate (1), the gate stack comprising a conductive layer (4_1) overlying the substrate (1); forming a bottom electrode conductive layer (4_2) over the conductive layer (4_1); forming a ferroelectric material layer (5) over

the bottom electrode layer (4_2); forming a top electrode conductive layer (6) over the ferroelectric material layer (5); forming drain and source regions (2) on opposite sides of the gate stack; and a dielectric spacer (8) on the sidewall of the gate stack (col. 4, line 63 thru col. 6, line 22). Willer et al. further disclose the formation of the gate stack comprising the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack (Fig.2; col. 5, lines 41-63).

Since Suzuki et al. and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al. would have been recognized in the pertinent art of Suzuki et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Suzuki et al. by a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer as taught by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Moon (5,744,374).

Suzuki et al. disclose the subject matter claimed above except wherein the formation of the gate stack comprised the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack.

Moon discloses a method of fabricating a ferroelectric transistor where a gate stack (20) is formed on a semiconductor substrate (1), the gate stack (20) comprising an oxide layer (11) overlying the substrate (1); forming a ferroelectric material layer (12)

over the oxide layer (11); forming a top electrode conductive layer (13) over the ferroelectric material layer (12); forming drain and source regions (9) on opposite sides of the gate stack (20).

Referring to claim 7, Moon further discloses the formation of the gate stack (20) comprising the deposition of the multilayer gate stack (20), the photolithography patterning (16) of the gate stack (20) and the etching of the gate stack (20) (col. 4, line 58 thru col. 5, line 33).

Referring to claim 8, Moon discloses wherein the formation of the drain and source regions (9) comprises an implantation to form a high doping concentration into the source and drain regions (9) (col.6, lines 25-34).

Referring to claim 9, Moon discloses wherein the formation of the drain and source regions (9) comprises an implantation to form a LDD ion implantation into the source and drain regions (9) (col.6, lines 25-34).

Referring to claim 10, Moon discloses a dielectric spacer (18) on the sidewall of the gate stack (20) (col. 6, lines 1-34).

Since Suzuki et al. and Moon are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Moon would have been recognized in the pertinent art of Suzuki et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Suzuki et al. by the formation of the gate stack comprised the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack as taught by Moon to decrease operation voltage (col. 2, lines 1-20).

Claims 13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Sakai et al. (2003/0067022).

Suzuki et al. disclose the subject matter claimed above except forming a replacement gate stack on the substrate, the replacement gate stack which includes a sacrificial layer; forming drain and source regions on opposite sides of the replacement gate stack; filling the area surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer portion of the replacement gate stack; forming the remainder of the gate stack.

Sakai et al. disclose a method of fabricating a ferroelectric transistor where a replacement gate stack is formed on a semiconductor substrate (1), the replacement gate stack comprising an oxide layer (40,3) overlying the substrate (1); and a sacrificial layer (42) over the oxide layer (40,3) (Fig. 4A); forming drain and source regions (7,8) on opposite sides of the replacement gate stack (Fig. 4B); filling the areas surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer (42) portion of the replacement gate stack (Fig. 4E); forming the remainder of the gate stack, the remainder of the gate stack comprising a ferroelectric material layer (45) and a top electrode conductive layer (46) (para. 94-100).

Since Suzuki et al. and Sakai et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Sakai et al. would have been recognized in the pertinent art of Suzuki et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify Suzuki et al. by forming a replacement gate stack on the substrate, the replacement gate stack which includes a sacrificial layer; forming drain and source regions on opposite sides of the replacement gate stack; filling the area surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer portion of the replacement gate stack; forming the remainder of the gate stack as taught by Sakai et al. to increase density and reduce cell area (para. 15).

Referring to claim 15, Sakai et al. disclose the sacrificial layer (42) comprising silicon nitride or silicon dioxide (para. 94, 99).

Referring to claim 16, Sakai et al. disclose depositing of a dielectric film (43); and the planarization of the deposited dielectric film (43) to expose the top portion of the replacement gate stack (Fig. 4C; 4D).

Referring to claim 17, Sakai et al. disclose forming the remainder of the gate stack by depositing the ferroelectric material layer (45), the planarization of the ferroelectric material layer (45), the deposition of the top electrode conductive layer (46); the photolithography patterning of the top electrode conductive layer (46), and the etching of the top electrode conductive layer (46) (para. 94-100).

Referring to claim 18, Sakai et al. disclose the formation of the replacement gate stack comprises the deposition of the replacement gate stack, the photolithography patterning of the replacement gate stack and the etching of the replacement gate stack (para. 94).

Referring to claim 19, Suzuki et al. disclose wherein the electrode conductive layer (43) is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide (col. 9, lines 29-60).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. in view of Sakai et al. as applied to claim 13 above, and further in view of Willer et al.

Suzuki et al. disclose the subject matter claimed above except a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a method of fabricating a ferroelectric transistor where a gate stack is formed on a semiconductor substrate (1), the gate stack comprising a conductive layer (4_1) overlying the substrate (1); forming a bottom electrode conductive layer (4_2) over the conductive layer (4_1); forming a ferroelectric material layer (5) over the bottom electrode layer (4_2); forming a top electrode conductive layer (6) over the ferroelectric material layer (5); forming drain and source regions (2) on opposite sides of the gate stack; and a dielectric spacer (8) on the sidewall of the gate stack (col. 4, line 63 thru col. 6, line 22). Willer et al. further disclose the formation of the gate stack comprising the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack (Fig.2; col. 5, lines 41-63).

Since Suzuki et al. and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al.

would have been recognized in the pertinent art of Suzuki et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Suzuki et al. by a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer as taught by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
27 December 2006

Zandra V. Smith
Supervisory Patent Examiner
29 Dec. 2006